ELECTRONIC CIRCUITS
LAB MANUAL

Hardware realization part

As per Calicut University Syllabus (2009)

Department of
Electronics and Communication Engineering
MEA Engineering College
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RECTIFIERS

Aim:
To study Half Wave and Full Wave Rectifiers and to calculate ripple factor and efficiency without using filters

Components and equipments required:

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<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
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<tbody>
<tr>
<td>1.</td>
<td>Diodes</td>
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<td>4 No</td>
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<tr>
<td>2.</td>
<td>Resistor</td>
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<td>Step down transformer (230V/6-0-6V), Cathode Ray Oscilloscope (CRO) with Probes, Connecting Board</td>
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Theory:
Rectifiers are a class of circuits whose purpose is to convert ac waveforms (usually sinusoidal and with zero average value) into a waveform that has a significant non-zero average value (dc component). Simply stated, rectifiers are ac-to-dc energy converter circuits.

Depending on the output, rectifiers are of two types:

a. Half wave (HW) rectifier,
b. Full wave (HW) rectifier

Half wave rectifier consists of only one diode, as shown in fig 1(a). In the half-wave rectification, during the positive half-cycle of the ac input, the diode is forward biased and it conducts current. During negative half-cycle, the diode is reverse biased and it does not conduct the current. So, in this rectifier only half of the wave is rectified. The output dc voltage shown in fig 1(b), its maximum efficiency is 40.6%.

A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output. Full-wave rectification converts both polarities of the input waveform to DC (direct current), and is more efficient. There are two types of full wave rectifier: Centre Tap FW rectifier and Bridge rectifier

In a CT Full Wave Rectifier circuit (figure 2(a)) two diodes are now used, one for each half of the cycle. A transformer is used whose secondary winding is split equally into two halves with a common centre tapped connection (C). When the input ac is switched on, during the positive half-cycle, the terminal 1 becomes positive and D1 is forward biased and it conducts current, and terminal 2 becomes negative and D2 is reverse biased and it does not conduct. During the negative half-cycle, the terminal 2 becomes positive, terminal 1 becomes negative and D2 is forward biased and it conducts current, terminal 1 becomes negative and D1 does not conduct. Therefore the two diodes work alternately. Hence the current flow through the load in both cycles will be in same direction. The output voltage waveform across the load is shown in fig 2(c). Its maximum efficiency is 81.2%.

In bridge rectifier circuit the single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown in figure. In this rectifier, four diodes (D1, D2, D3 and D4) are connected as a bridge, as shown in the fig 2(b). During the positive half cycle of the input sine wave terminal 1 becomes positive and D2 become negative. So D1and D3 are forward biased and they conduct current, and D2 and D4 are reverse biased and they do not conduct. During the negative half-cycle, the terminal 2 becomes positive, terminal 1 becomes negative and D2 and D4 are for-ward biased and they conduct current, and D1 and D3 are
reverse biased and they do not conduct. Therefore the two pairs of diodes work alternately (as in fig 2(c)). So the complete wave is rectified.

**Circuit Diagram and Waveforms:**

![Half wave rectifier](image1)

**Fig 1(a). Half wave rectifier**

![Center Tap Full wave rectifier](image2)

**Fig 2(a). Center Tap Full wave rectifier**

![Bridge Rectifier](image3)

**Fig 2(b). Half wave rectifier waveforms**

![Bridge Rectifier](image4)

**Fig 2(c). Full wave rectifier waveforms**

**Procedure:**

1. Connections are made as shown in the circuit diagram
2. Switch on the AC power supply
3. Observe the wave form on CRO across the load resistor and measure the o/p amplitude and frequency.
4. Calculate the r. m. s voltage value, d. c. output voltage, ripple factor and efficiency.
Half wave rectifier:

The r.m.s value of the load voltage: $V_{\text{rms}} = \frac{V_m}{2}$, where $V_{\text{m(input)}}$ is the peak value of the output voltage.

Similarly $I_m = \frac{V_m}{(R_L + r_f)}$ and $I_{\text{rms}} = \frac{I_m}{2}$, where $r_f \ll R_L$, is the forward resistance of the diode.

D.C (or average) value: $V_{\text{dc}} = \frac{V_m}{\pi}$, $I_{\text{dc}} = \frac{I_m}{\pi}$

Ripple factor, $\gamma = \frac{\text{Ripple Voltage}}{\text{D.C Voltage}} = \frac{\text{rms value of a.c component}}{\text{Average or d.c component}} = \frac{\sqrt{I_{\text{rms}} - I_{\text{dc}}}}{I_{\text{dc}}} = 1.21$ (theoretical)

Efficiency, $\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} = \frac{(I_{\text{dc}})^2 \times R_L}{(I_{\text{rms}})^2 (r_f + R_L)} = 0.406$ (theoretical).

Full wave rectifier:

The r.m.s value of the input voltage: $V_{\text{rms}} = \frac{V_m}{\sqrt{2}}$, where $V_{\text{m(input)}}$ is the peak value of transformer secondary voltage.

Similarly $I_m = \frac{V_m}{(R_L + r_f)}$, and $I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$, where $r_f \ll R_L$, is the forward resistance of the diode.

D.C (or average) value: $V_{\text{dc}} = 2 \frac{V_m}{\pi}$, $I_{\text{dc}} = 2 \frac{I_m}{\pi}$

Ripple factor, $\gamma = \frac{\text{Ripple Voltage}}{\text{D.C Voltage}} = \frac{\text{rms value of a.c component}}{\text{Average or d.c component}} = \frac{\sqrt{I_{\text{rms}} - I_{\text{dc}}}}{I_{\text{dc}}} = 0.482$ (theoretical)

Efficiency, $\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} = \frac{(I_{\text{dc}})^2 \times R_L}{(I_{\text{rms}})^2 (r_f + R_L)} = 0.812$ (theoretical).

Tabular Column:

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<th>Rectifier</th>
<th>$V_m$</th>
<th>$V_{\text{rms}}$</th>
<th>$V_{\text{dc}}$</th>
<th>$I_{\text{rms}}$</th>
<th>$I_{\text{dc}}$</th>
<th>$I_{\text{rms}}$</th>
<th>$\gamma$</th>
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</table>

Result:
FILTERS

Aim:
To study Half Wave and Full wave Rectifiers and to calculate ripple factor, efficiency and regulation with C, LC and CLC filters.

Components and equipments required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
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<th>Qty</th>
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<td>1.</td>
<td>Diodes</td>
<td>1N4007</td>
<td>4</td>
</tr>
<tr>
<td>2.</td>
<td>Capacitors</td>
<td>*as per design</td>
<td>3</td>
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<tr>
<td>3.</td>
<td>Inductor</td>
<td>*as per design</td>
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Step down transformer (230V/6-0-6V), Cathode Ray Oscilloscope (CRO) with Probes, Connecting Board

Theory:

It is necessary to include a filter between the rectifier and the loads in order to eliminate the ripple components in the output of rectifier. The most commonly used filter circuits are 1) Shunt capacitor filter 2) Series inductor filter 3) Choke in put filter or L- filter and 4) Capacitor in put filter or π –filter.

**Shunt capacitor filter:** - The shunt capacitor filter is obtained by placing a capacitor C in parallel with a load resistor R_L. The capacitor C is so chosen that its reactance (1/\omega C) at the frequency of a.c. main is very small as compared to the load R_L. Then the a.c components find a low reactance shunt path through the capacitor and are mostly bypassed. Thus, the a.c components or ripples flowing through the load decrease or in other words ripples are filtered from the output voltage. The ripple factor in capacitor filter is given by \gamma = 1/4\sqrt{3fCR_L}.

**Series inductor filter:** - The series inductor filter is obtained by placing an inductor coil (L) in series with a load resistor RL. The inductor stores energy as magnetic energy, when the current is above its average value and delivers that energy to the circuit when the current tends to fall below the average level. Thus, it reduces the pulsation of the rectifier output. The ripple factor in series inductor filter \gamma = R_L/3\sqrt{2\omega L}.

**LC (Choke input) filter or:** - To meet the demand for the lower ripple factors, series inductor and shunt capacitor are combined together to give LC filter. In this filter the series inductor passes the d.c components from the rectifier output but introduces the high reactance (\omega L) path for a.c. The a.c components that remain after passing through the inductor are bypassed by the shunt capacitor C which offers a low reactance (1/\omega C) to them, but infinite resistance to d.c. Thus the output across the load R_L possesses less a.c. component or the low ripple factor. The ripple factor of a chock input filter is given by \gamma = 1.194 \times 10^{-6}/LC (by taking f=50Hz).

**Bleeder resistor**
For optimum functioning, the inductor requires a minimum current to flow through, at all time. When the current falls below this rat, the output will increase sharply and hence the regulation become poor. To keep up the circuit current above this minimum value, a resistor is permanently connected across the filtering capacitor and is called bleeder resistor. This resistor always draws a minimum current even if the external load is removed. It also provides a path for the capacitor to discharge when power supply is turned off.
**CLC (π-) filter:** - When higher output voltage at light loads is desired, an input capacitor C1 is added to LC filter to form a π-filter. The use of π-filter provides an output voltage that approaches the peak value of the a.c potential of the source, the ripple components being very small. In this case ripple factor, 

\[ \gamma = \sqrt{2} \frac{X_{C1}X_{C2}}{X_LR_L}. \]

**Circuit Diagram:**

![Fig 1. Shunt Capacitor Filter](image1)

![Fig 2. Series Inductor Filter](image2)

![Fig 3. LC Filter](image3)

![Fig 4. CLC Filter](image4)
Waveforms

Design (For Given Load \(R_L\) and ripple \(\gamma\)): 

\[ R_L = \frac{V_{dc}}{I_{dc}}, \quad \text{where} \quad V_{dc} \quad \text{and} \quad I_{dc} \quad \text{are the dc output requirements} \]

1. Capacitor Filter:
   
   Given, 
   
   Ripple \(\gamma = 0.06, f = 50Hz\)
   
   We have \(C_1 = \frac{1}{4\sqrt{3} \cdot f \cdot \gamma \cdot R_L} = \frac{1}{4\sqrt{3}(50)(0.06)R_L} = \frac{0.0481}{R_L} \quad \text{F} \)

2. L Filter
   
   Given Ripple \(\gamma = 0.06, f = 50Hz\)
   
   We have \(L_1 = \frac{R_L}{3\sqrt{2} \cdot \omega \cdot \gamma \cdot R_L} = \frac{1}{3\sqrt{2}(2\pi \times 50)(0.06)R_L} = \frac{0.125}{R_L} \quad \text{H} \)

3. LC Filter
   
   Given Ripple \(\gamma = 0.06, f = 50Hz\)
   
   \(\gamma = 1.19410^{-6}/L_1 C_1\).
   
   Choose a standard inductor \(L\), and then find \(C\) using the above equation.

4. CLC Filter
   
   We have \(\gamma = \sqrt{2} X_{C1} X_{C2}/X_L R_L\), Ripple \(\gamma = 0.06, f = 50Hz\)
   
   Let \(C_1 = C_2 = C\) then \(X_{C1} = X_{C2} = 1/\omega C\), then \(\gamma = \frac{\sqrt{2}}{8\pi^3 \times 50^3 C^2 L} = \frac{4.47 \times 10^{-8}}{C^2 L}\), where \(C\) in Farad and \(L\) in Henry.
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Procedure:

1. Check and verify all the given components are in good condition.
2. Wire the circuits as per the circuit diagram.
3. Check the outputs of the rectifier circuits before connecting the filter circuit,
4. Connect the filter circuit, and verify the outputs.

Result:
CLAMPING CIRCUITS

Aim:

Design a clamping circuit for the given output.

Components and equipments required:

<table>
<thead>
<tr>
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<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Diodes</td>
<td>1N4007</td>
<td>2 No</td>
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<tr>
<td>2.</td>
<td>Capacitors</td>
<td>0.1 μF or 1 μF</td>
<td>1 No</td>
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<tr>
<td>3.</td>
<td>Resistors</td>
<td>3.3kΩ</td>
<td>1 No</td>
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Signal generator, Cathode Ray Oscilloscope (CRO) with Probes, Dual Power Supply, Connecting Board

Theory:

A clamper is one, which provides a D.C shift to the input signal. The D.C shift can be positive or negative. The clamper with positive D.C shift is called positive clamper and clamper with negative shift is called negative clamper. Consider a clamper circuit shown below.

In the positive half cycle as the diode is forward biased the capacitor charges to the value $V_{IN} - V_{D+}$ with the polarity as shown in the figure. In the negative half cycle the diode is reverse biased. Hence the output is $V_{O} = V_{IN} - V_{C}$. Initially let us assume that the capacitor has charged to $V_{IN} = (10 - 0.6) = 9.4$ V.

Then in the positive half cycle diode is forward biased and applying KVL to the loop,

\[ V_{in} = V_{C} - V_{o} = 0 \]

\[ V_{o} = V_{in} - V_{C} \]

When $V_{in} = 0$, $V_{o} = 0 - 9.4 = -9.4$ V

$V_{in} = 10$ V, $V_{o} = 10 - 9.4 = 0.6$ V

In the negative half cycle,

When $V_{in} = -10$ V  $V_{o} = -10 - 9.4 = -19.4$ V

The output shifts between 0.6 V and –19.4 V. Here the output has shifted down by 9.4 V. The peak to peak voltage at the output of a clamper is the same as that of the input.
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Circuit Diagram and Design and Waveforms:

Given \( V_{in} = 20 \text{V (p-p)} \)

A. **Negative Clamper at 0V**

**In the positive half cycle:**
Diode is forward biased.
Applying KVL to loop 1
\[
V_{in} - V_C - V_D = 0
\]
\[
V_C = V_{in} - V_D = 10 - 0.6 = 9.4 \text{V}
\]

In the negative half cycle:
\[
V_{in} - V_C - V_0 = 0
\]
\[
V_0 = V_{in} - V_C
\]
When \( V_{in} = 0 \), \( V_0 = -9.4 \text{V} \)
When \( V_{in} = 10 \text{V} \), \( V_0 = 0.6 \text{V} \)
When \( V_{in} = -10 \text{V} \), \( V_0 = -19.4 \text{V} \)

B. **Positive Clamper at 0V**

**In the negative half cycle:**
Diode is forward biased.
Applying KVL to loop 1
\[
V_{in} + V_C + V_D = 0
\]
\[
V_C = -(V_{in} + V_D)
\]
\[
V_C = -(10 + 0.6)
\]
\[
= -9.4 \text{V}
\]

**In the positive half cycle:**
Diode is reverse biased.
Apply KVL to the loop
\[
V_{in} + V_C - V_0 = 0
\]
\[
V_0 = V_{in} + V_C
\]
When \( V_{in} = 0 \), \( V_0 = 9.4 \text{V} \)
When \( V_{in} = 10 \text{V} \), \( V_0 = 10 + 9.4 = 19.4 \text{V} \)
C. Negative Clamper at \( +V_R \) volts.
Assume \( V_R = 2V \)

**In the positive half cycle:**
- Diode is forward biased.
- Apply KVL to loop 1
  \[
  V_{in} - V_C - V_D - V_R = 0
  \]
  \[
  V_C = V_{in} - V_D - V_R
  \]
  \[
  = 10 - 0.6 - 2
  \]
  \[
  = 7.4V
  \]

**In the negative half cycle:**
- Diode is reverse biased
- \( V_{in} - V_C - V_0 = 0 \)
- \( V_0 = V_{in} - V_C \)
- When \( V_{in} = 0V \) \( V_0 = -7.4V \)
- When \( V_{in} = 10V \) \( V_0 = 2.6V \)
- When \( V_{in} = -10V \) \( V_0 = -17.4V \)

---

D. Negative Clamper at \( -V_R \) volts.
Assume \( V_R = 2V \)

**In the positive half cycle:**
- Diode is forward biased and the capacitor charges.
- Apply KVL to loop 1
  \[
  V_{in} - V_C - V_D + V_R = 0
  \]
  \[
  V_C = V_{in} - V_D + V_R = 10 -0.4 +2 = 11.4V
  \]

**In the negative half cycle:**
- \( V_{in} - V_C - V_0 = 0 \)
- \( V_0 = V_{in} - V_C \)
- When \( V_{in} = 0V \) \( V_0 = -11.4V \)
- When \( V_{in} = 10V \) \( V_0 = -1.4V \)
- When \( V_{in} = -10V \) \( V_0 = -21.4V \)
E. Positive Clamper at $+V_R$ volts.
Assume $V_R = 2V$

**In the negative half cycle:**
Assume $V_R = 2V$
Diode is forward biased and capacitor charges.
Apply KVL to the loop 1
\[ V_{in} + V_C + V_D + V_R = 0 \]
\[ V_C = -(V_{in} + V_R + V_D) \]
\[ = -(10 + 0.6 + 2) = 7.4V \]

**In the positive half cycle:**
From the fig. we see that
\[ V_{in} + V_C - V_0 = 0 \]
\[ V_0 = V_{in} + V_C \]
When $V_{in} = 0$ $V_0 = 7.4V$
When $V_{in} = 10V$ $V_0 = 17.4V$
When $V_{in} = -10V$ $V_0 = -2.6V$

F. Positive Clamper at $-V_R$ volts.
Assume $V_R = 2V$

**In the negative half cycle:**
Diode is forward biased and capacitor charges.
Apply KVL to loop 1
\[ V_{in} + V_C + V_D - V_R = 0 \]
\[ V_C = -(V_{in} + V_R - V_D) \]
\[ = -(10 + 0.6 - 2) \]
\[ = 11.4V \]

**In the positive half cycle:**
From the circuit we see that,
\[ V_{in} + V_C - V_0 = 0 \]
\[ V_0 = V_{in} - V_C \]
When $V_{in} = 0V$ $V_0 = 11.4V$
When $V_{in} = 10V$ $V_0 = 21.4V$
When $V_{in} = -10V$ $V_0 = 1.4V$
Procedure:

1. Wire up the circuit as shown in the circuit diagram.
2. Give a sinusoidal input of 20 V peak to peak.
3. Check and verify the output on CRO.

Result:
CLIPPING CIRCUITS

**Aim:**

Design a clipping circuit for the given values.

**Components Required:**

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
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<td>1.</td>
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Signal Generator, Dual power supply, CRO, etc.

**Theory:**

The process by which the shape of a signal is changed by passing the signal through a network consisting of linear elements is called linear wave shaping. Most commonly used wave shaping circuit is clipper. Clipping circuits are those, which cut off the unwanted portion of the waveform or signal without distorting the remaining part of the signal.

The basic components required for a clipping circuit are – an ideal diode and a resistor. In order to fix the clipping level to the desired amount, a dc battery must also be included. When the diode is forward biased, it acts as a closed switch, and when it is reverse biased, it acts as an open switch. Different levels of clipping can be obtained by varying the amount of voltage of the battery and also interchanging the positions of the diode and resistor.

Depending on the features of the diode, the positive or negative region of the input signal is “clipped” off and accordingly the diode clippers may be positive or negative clippers.

There are two general categories of clippers: series and parallel (or shunt). The series configuration is defined as one where diode is in series with the load, while the shunt clipper has the diode in a branch parallel to the load.
Circuit Diagram and Design:

A. Series Clipper
   a. Negative Clipper at 0V
      
      Assume $V_{in} = 10V$ (Peak to Peak)
      
      In the positive half cycle D is forward biased
      
      \[ V_0 = V_{in} - 0.6 = 5 - 0.6 = 4.4 \] (0.6V is the diode drop)
      
      In the negative half cycle D is reverse biased
      
      \[ V_0 = 0V \]

   b. Positive Clipper at 0V
      
      In the positive half cycle D is reverse biased
      
      \[ V_0 = 0V \]
      
      In the negative half cycle D is forward biased,
      
      Applying KVL to the loop
      
      \[ V_{in} + V_D - V_0 = 0 \]
      
      \[ V_0 = V_{in} + V_D = -5 + 0.6 = -4.4V \]

   c. Negative clipper with positive reference voltage
Given $V_R = 2.5V$

In the **positive half cycle**
(i) When $|V_{in}| > |V_D + V_R|$, D is forward biased

Applying KVL, we get

$V_{in} = V_D + V_R + V_0$

$V_0 = V_{in} - V_D - V_R$

$V_0 = 5 - 0.5 - 2.5$

$V_0 = 2V$

(ii) When $|V_{in}| < |V_D + V_R|$, D is reverse biased

$V_0 = 0V$

In the **negative half cycle**, D is reverse biased

$V_0 = 0V$

---

d. **Positive clipper with negative reference voltage**

Assume $V_R = 3V$

In the **positive half cycle**, D is reverse biased

$V_0 = 0V$

In the **negative half cycle**, D is reverse biased

$V_0 = 0V$

(i) When $|V_{in}| > |V_D + V_R|$, D is forward biased.

Applying KVL, we get

$V_{in} = -V_D - V_R + V_0 \implies V_0 = V_{in} + V_D + V_R$

$V_0 = -5 + 0.6 + 3$

$V_0 = -1.5V$

---

e. **Dual clipper.**
Assume $V_{R1} = 2.5V$ and $V_{R2} = 3V$

In the **positive half cycle**, $D_1$ is reverse biased

(i) When $|V_{in}| > |V_{D1} + V_{R1}|$, $D_1$ is forward biased

Applying KVL, we get

\[
V_{in} = V_{D1} + V_{R1} + V_0
\]
\[
V_0 = V_{in} - V_{D1} - V_{R1}
\]
\[
V_0 = 5 - 0.6 - 2.5
\]
\[
V_0 = 2V
\]

(ii) When $|V_{in}| < |V_{D1} + V_{R1}|$, $D_1$ is reverse biased

$V_0 = 0V$

In the **negative half cycle**

(i) When $|V_{in}| > |V_{D2} + V_{R2}|$, $D_2$ is forward biased

Applying KVL, we get

\[
V_{in} = -V_{D} - V_{R} + V_0
\]
\[
V_0 = V_{in} + V_{D2} + V_{R2}
\]
\[
V_0 = -5 + 0.6 + 3
\]
\[
V_0 = -1.5V
\]

(ii) When $|V_{in}| < |V_{D2} + V_{R2}|$, $D_2$ is reverse biased

$V_0 = 0V$

**B. Shunt Clipper**

**a. Negative Clipper at 0V (neglecting the diode drop)**

During the **positive half cycle**, $D$ is forward biased

$V_0 = V_D = 0.6V$

During the **negative half cycle**, $D$ is reverse biased

$V_0 = V_{in}$
b. Positive Clipper at 0V (neglecting the diode drop)

During positive half cycle, D is reverse biased
\[ V_0 = V_{in} \]

During negative half cycle, D is forward biased
\[ V_0 = -V_D = -0.6V \]

\[
\begin{align*}
\text{Positive Clipper at } &0V \\
&\text{(neglecting the diode drop)}
\end{align*}
\]

\[
\begin{align*}
\text{During positive half cycle, } D &\text{ is reverse biased} \\
V_0 &= V_{in} \\
\text{During negative half cycle, } D &\text{ is forward biased} \\
V_0 &= -V_D = -0.6V \\
\end{align*}
\]

c. Positive clipper at +3V

\[
\begin{align*}
\text{During positive half cycle} \\
&\text{(i) When } |V_{in}| > |V_D + V_R|, \ D \text{ is forward biased} \\
V_0 &= V_D + V_R = 0.5 + 2.5 \\
V_0 &= 3V \\
&\text{(ii) When } |V_{in}| < |V_D + V_R|, \ D \text{ is reverse biased} \\
V_0 &= V_{in} \\
\end{align*}
\]

During negative half cycle, D is reverse biased
\[ V_0 = V_m \]
d. Negative clipper at -3V

During positive half cycle, D is reverse biased
\[ V_0 = V_n \]

During negative half cycle
(i) When \(|V_n| > |V_D + V_R|\), D is forward biased, applying KVL to the loop, we get
\[ V_0 = -V_D - V_R = -0.6 - 2.5 = -3V \]

(ii) When \(|V_n| < |V_D + V_R|\), D is reverse biased
\[ V_0 = V_n \]

e. Positive clipper at -3V

During positive half cycle, D is forward biased, applying KVL
\[ V_0 = V_D - V_R = 0.6 - 3.6 = -3.0V \]

During the negative half cycle
(i) When \(|V_n| < |(V_D - V_R)|\), D is forward biased, Applying KVL to the loop, we get
\[ V_0 = V_D - V_R = 0.6 - 3.6 = -3.0V \]

(ii) When \(|V_n| > |(V_D + V_R)|\), D is reverse biased
\[ V_0 = V_n \]
Electronic Circuit Lab Manual

f. Negative clipper at +3V

During negative half cycle, D is forward biased, Applying KVL
\[ V_0 = -V_D + V_R = -0.6 + 3.6 = 3.0V \]

During the positive half cycle
(i) When \( V_m < (-V_D + V_R) \), D is forward biased, Applying KVL to the loop, we get
\[ V_0 = -V_D + V_R = -0.6 - 2.5 = -3.0V \]
(ii) When \( V_m > (V_D + V_R) \), D is reverse biased
\[ V_0 = V_m \]

Assume \( |V_{R1}| = |V_{R2}| = 2.4V \)

During positive half cycle, \( D_2 \) is reverse biased,
(i) When \( |V_m| > |V_{D1} + V_{R1}| \), \( D_1 \) is forward biased
\[ V_0 = V_{D1} + V_{R1} = 0.6 + 2.4 \quad \text{(by KVL)} \]
\[ V_0 = 3V \]
(ii) When \( |V_m| < |V_{D1} + V_{R1}| \), \( D_1 \) is reverse biased
\[ V_0 = V_m \]

During negative half cycle, \( D_1 \) is reverse biased
(i) When \( |V_m| > |V_{D2} + V_{R2}| \), \( D_2 \) is forward biased, applying KVL to the loop, we get
\[ V_0 = -V_{D2} - V_{R2} = -0.6 - 2.4 \]
\[ V_0 = -3V \]
(ii) When \( |V_m| < |V_{D2} + V_{R2}| \), \( D_2 \) is reverse biased,
\[ V_0 = V_m \]
h. Slicer. (clipping levels at \( +V_{R1} \) and \( +V_{R2} \) volts)

Assume \( V_{R1} = V_{R2} = 2V \).

**During positive half cycle**

(i) When \(|V_{in}| < |V_{R2} - V_{D2}|\), \(D_1\) is reverse biased and \(D_2\) is forward biased

\[
V_0 = -V_{D2} + V_{R2} = -0.6 + 2 \rightarrow 1.4V
\]

(ii) When \(|V_{in}| > |V_{D1} + V_{R1}|\), \(D_1\) is forward biased and \(D_2\) is reverse biased

\[
V_0 = V_{D1} + V_{R1} = 0.6 + 2 = 2.6V
\]

**During negative half cycle**, \(D_1\) is reverse biased and \(D_2\) is forward biased

\[
V_0 = -V_{D2} + V_{R2} = -0.6 + 2 \rightarrow V_0 = 1.5V
\]

**Procedure:**

1. Rig up the circuit as shown in the fig.
2. Give a sinusoidal input of 10V peak to peak.
3. Check the output at the output terminal.
4. To plot the transfer characteristics, connect channel 1 of the CRO to the output and channel 2 to the input and press the XY knob.
5. Adjust the grounds of both the channels to the centre.
6. Measure the designed values.

**Result:**


**JFET CHARACTERISTICS**

**Aim:**
To plot the characteristics of a JFET and to calculate its parameters

**Components and equipments required:**

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BFW10</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>1kΩ</td>
<td>2 No</td>
</tr>
<tr>
<td></td>
<td>DC power supply(s), voltmeters, ammeters, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Theory:**
JFET is a unipolar device because its function depends on only upon the type of carrier. JFET has high input impedance unlike BJT. JFETSs are of two types N-Channel and P-Channel. An N-Channel JFET is an N-type silicon bar with a P-type semiconductor embedded on both sides of the bar. P-type semiconductor forms the gate and the ends of N-type bar are source and drain. The P regions are internally shorted. The gate of an N channel JFET is connected to a negative potential with respect to source and the drain is connected to a positive potential with respect to source.

**Drain dynamic resistance** $r_d$, it is defined as the ratio of change in drain to source voltage to the change in drain current, when gate to source voltage remains constant.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ with } V_{GS} \text{ constant.}$$

**Mutual Conductance** $g_m$: It is defined as the ratio of change in drain current to the change in gate to source voltage, when drain to source voltage remains constant.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ with } V_{DS} \text{Constant}$$

**Amplification factor** $\mu$: It is defined as the ratio of change in drain to source voltage to the change in gate to source voltage, when the drain current remains constant.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ with } I_D \text{ constant}$$

$\mu, g_m$ and $r_d$ are related each other by the expression

$$\mu = g_m \times r_d$$

**Procedure:**
1. Identify the terminals of FET, wire up the ckt on the bread board.
2. Switch on $V_{GS}$ and $V_{DS}$ supplies keeping rheostat in minimum position. Fix $V_{GS}$ at 0v. Increase $V_{DS}$ in steps and note down the drain current $I_D$ for each value of $V_{DS}$. Repeat it for different values of $V_{GS}$ say 1v and 2v.
3. Plot ‘drain’ characteristics with $I_D$ along Y axis and $V_{DS}$ along X axis.
4. Keep $V_{DS}$ = 10V. Vary $V_{GS}$ and note down the values of $I_D$ for different values of $V_{GS}$. Plot the mutual characteristics ($V_{GS}$ along X and $V_{DS}$ along Y axis). Repeat this step for $V_{DS}$ = 20V.
5. Calculate FET parameters using their formulas.
Observations and drain characteristics:

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$V_{DS}$ (V)</th>
<th>$I_D$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>-1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Observations and transfer characteristics:

<table>
<thead>
<tr>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}$ (V)</th>
<th>$I_D$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Quick reference data of BFW10

<table>
<thead>
<tr>
<th>Number</th>
<th>Type</th>
<th>$I_D$</th>
<th>$g_m$</th>
<th>$r_o$</th>
<th>$V_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td>BFW10</td>
<td>N-channel</td>
<td>2mA</td>
<td>2.5mA/V</td>
<td>40k</td>
<td>8V</td>
</tr>
</tbody>
</table>

Result:

- Dynamic drain resistance $r_d =$ ............
- Mutual conductance $g_m =$ ............
- Amplifier factor $\mu =$ ............
MOSFET CHARACTERISTICS

Aim
To study and plot the MOSFET Characteristics

Components and equipments required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BS170</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>1kΩ</td>
<td>2 No</td>
</tr>
<tr>
<td></td>
<td>DC power supply(s), voltmeters, ammeters, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory:
MOSFETs are three terminal devices having a source gate and a drain. MOSFET is the abbreviation of Metal Oxide Semiconductor Field Effect Transistor. It uses a thin layer of silicon dioxide as an insulator between the gate and the channel. It is also known as Insulated Gate Field Effect Transistor (IGFET).

There are two types of MOSFET, depletion and enhancement types. Consider the N-Channel depletion type MOSFET. Heavily doped two N-Type regions are diffused on a lightly doped P-Type substrate to form source and drain. Between these two N Type wells a lightly doped N-Type material forms a channel. A thin layer of SiO₂ which is an insulating material is fabricated on the surface above the channel and the gate terminal is attached to it. Source and Drain terminals are attached to the heavily doped N-Type material with metal contacts.

A positive voltage $V_{DS}$ is applied at the drain with respect to source to establish drain current. When a negative voltage $V_{GS}$ is applied at the gate with respect to the source, positive charges get induced in the channel resulting the channel becoming effectively thinner. This reduces the current flow through the channel. If the magnitude of $V_{GS}$ is increased, the drain current decreases. If a positive voltage is applied at the gate, drain current increases.

Enhancement type MOSFET does not have a channel fabricated in it. The applied positive voltage induces negative charges between the source and drain and a channel forms. BS170 is a low power enhancement type MOSFET. Some MOSFETs are able to function in Enhancement and Depletion modes.

Construction of MOSFET:

Quick reference data of BFW10

<table>
<thead>
<tr>
<th>Number</th>
<th>$V_{DS}$</th>
<th>$V_{GS}$</th>
<th>$I_D$</th>
<th>$P_D$</th>
<th>$g_{m}$</th>
<th>$R_{DS, on}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>BFW10</td>
<td>60V</td>
<td>±20V</td>
<td>500mA</td>
<td>350mW</td>
<td>200mho</td>
<td>5Ω</td>
</tr>
</tbody>
</table>
Procedure (Drain Characteristics):

1. Setup the circuit
2. Keep $V_{GS}$ at 0V. Vary $V_{DS}$ in equal steps and note down $I_D$. Repeat it for values of $V_{GS}$ at 2V and 4V.
3. Reverse the polarity of $V_{GS}$ and the voltmeter measuring it. Note down $I_D$ for negative values of $V_{DS}$, -2V and -4V. Plot a graph with $V_{DS}$ along x axis and $I_D$ along y axis.

Procedure (Mutual Characteristics):

1. Fix $V_{DS}$ at 10V. Note down drain current $I_D$ for various values of $V_{GS}$. Plot a graph with $V_{GS}$ along x axis and $I_D$ along y axis.

Observations and drain characteristics:

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$V_{DS}$ (V)</th>
<th>$I_D$ (mA)</th>
<th>$V_{GS}$ (V)</th>
<th>$V_{DS}$ (V)</th>
<th>$I_D$ (mA)</th>
<th>$V_{GS}$ (V)</th>
<th>$V_{DS}$ (V)</th>
<th>$I_D$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1V</td>
<td></td>
<td></td>
<td>2V</td>
<td></td>
<td></td>
<td>4V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Observations and transfer characteristics:

<table>
<thead>
<tr>
<th>$V_{DS1}$</th>
<th>$V_{DS2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS}$ (V)</td>
<td>$I_D$ (mA)</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Result:
CHARACTERISTICS OF UJT

Aim
To plot the VI characteristics of a unijunction transistor and to measure its intrinsic stand off ratio

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>UJT</td>
<td>2N2646</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>1kΩ, 10kΩ</td>
<td>2 No</td>
</tr>
<tr>
<td></td>
<td>DC power supply, CRO, Voltmeters, Ammeters, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory
A unijunction transistor consists of a bar of highly doped N Type semi conductor to which a heavily doped P Type rod is attached ohmic contacts are made at opposite ends of the N Type bar which are called base1 (B₁), base2 (B₂) of the transistor. P Type rod is called the emitter.

Refer to the equivalent circuit of the UJT given in figure. R₂ and R₁ are the resistances of B₁ and B₂ respectively. The intrinsic stand off ratio η is given by the expression

\[ η = \frac{R_{B1}}{R_{B1} + R_{B2}} \]

with \( I = 0 \)

Due to the applied voltage \( B₂ \) the transistor a positive voltage gets developed across \( R_{B1} \) and is equal to \( η V_{BB} \) if the voltage at the emitter \( V_E \) is less than the voltage across \( R_{B1} \) PN Junction remains reverse biased. If the emitter voltage \( V_E \) is increased above a level called peak voltage \( V_p = η V_{BB} + V_D \), a forward current flows through the emitter to B₁ region, \( V_D \) is the voltage drop across the pn junction. A current through \( R_{B1} \) results in the reduction of its resistance due to the negative coefficient of resistance of the semi conductor. Reduction in the \( R_{B1} \) causes an increase in current through it. This further reduces \( R_{B1} \) and so forth. After a particular value of \( V_E \), called valley point \( V_v \), emitter current increases with \( V_E \) similar to that of an ordinary forward biased diode. The region in the graph where current decreases with increase in current is called negative resistance region. This property of UJT is utilized in the relaxation oscillator.

Circuit Diagram:

```
+-----------------+      +-----------------+      +-----------------+
|                 |      |                 |      |                 |
| R1  10k          |      | IE              |      | Q1  2N2646      |
|                 |      | V1  10V         |      |                 |
| Q2  2N2646       |      | V2  0-30V       |      | VBB 0-30V       |
|                 |      |                 |      | V2  30V         |
```

Procedure:
1. Identify the leads of UJT correctly and set up the circuits as shown in figure.
2. Keeping \( V_{in} = 0 \), vary \( V_E \) from 0V to 10V in steps of 0.5V. Take the voltmeter and ammeter readings at the input side and enter it in tabular column. Repeat it for other values of \( V_{in} \) (say 3V & 6V)
3. Plot the VI characteristics with \( I_E \) along x-axis and \( V_E \) along x-axis.
4. Calculate the intrinsic stand off ratio from the graph using its expression.

Note: Since peak current \( I_p \) is in µA, initial rise of voltage in the graph may not be observable.
Pin out and Equivalent circuit of UJT (2N2646):

Details of 2N2646

<table>
<thead>
<tr>
<th>Number</th>
<th>( I_E )</th>
<th>( \eta )</th>
<th>( I_P )</th>
<th>( I_V )</th>
<th>( R_{BB} )</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>2n2646</td>
<td>2A</td>
<td>0.56-0.78</td>
<td>1.5µA</td>
<td>6mA</td>
<td>4.7kΩ to 9.1kΩ</td>
<td>TO 106</td>
</tr>
</tbody>
</table>

Observation and VI characteristics:

<table>
<thead>
<tr>
<th>( V_{BB} = 0V )</th>
<th>( V_{BB} = 3V )</th>
<th>( V_{BB} = 6V )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_E (V) )</td>
<td>( I_E (mA) )</td>
<td>( V_E (V) )</td>
</tr>
</tbody>
</table>

Result:

\[
\eta = \frac{V_P - V_D}{V_{BB}}
\]
UJT RELAXATION OSCILLATOR

Aim:
To design and set up a UJT Relaxation Oscillator.

Components and Equipments Required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>UJT</td>
<td>2N2646</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>1kΩ, 10kΩ</td>
<td>2 No</td>
</tr>
<tr>
<td></td>
<td>DC power supply, CRO, Voltmeters, Ammeters, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory:
UJT is a uni-polar device. The UJT is constructed using an N Type silicon bar on which P Type material is doped. It has three terminals base 1 (B₁), base 2 (B₂) and Emitter (E). An RC Circuit in association with UJT will function as a relaxation oscillator. The sharp pulse available from circuit can used to trigger SCRs.

Once the power supply is switched ON, Capacitor C is charged through resistor R towards $V_{BB}$. When the potential across the capacitor is $V_p$, UJT turns ON, and it enters in negative resistance region. Capacitor rapidly discharges through UJT since it then offers very slow resistance. This sudden discharge develops a sharp pulse at B₁. While discharging, when the capacitor voltage reaches valley voltage of UJT, it turns OFF. This enables the capacitor to charge again and repeat cycle.

The frequency of oscillation is given by,

$$f = \frac{1}{2\pi RC \log_e(\frac{1}{q})}$$

Procedure:
1. Wire up the circuit after testing the components and verifying the terminals of the UJT.
2. Switch ON the power supply and observe the waveforms at three terminals of the UJT on the CRO screen.
3. Vary the potentiometer for the fine adjustments of frequency.
**Design:**

**Output requirements:** Amplitude of the sweep waveform $V_p=10V$ and frequency=1KHz.

DC bias conditions: $V_{BB} = V_p / \eta = 10V/0.65 = 15V$.

**Details of 2N2646 as per data sheet:** $\eta=0.56$ to 0.75, typically $\eta =0.63$, $V_V = 1.5V$, $I_p = 5\mu A$ and $I_v = 4mA$.

**Design of R and C:** $R$ must be selected between $R_{\text{max}}$ and $R_{\text{min}}$.

- $R_{\text{max}} = (V_{BB} - V_P) / I_P = (15 - 10) / 15 \mu A = 1M\Omega$.
- $R_{\text{min}} = (V_{BB} - V_V) / I_v = (15 - 10) / 4 \mu A = 3.3k\Omega$.

Take GP of $R_{\text{max}}$ and $R_{\text{min}}$, i.e.,

$$R = \sqrt{1M\Omega \times 3.3k\Omega} = 57.40k\Omega.$$

Use $100k\Omega$ in series with $10k\Omega$ resistor.

We know that,

$$f = \frac{1}{R \times C \log_e \left(\frac{1}{\eta}\right)} = 1kHz.$$ 

So, $T = 1mS = 100 \times 10^3 \times C \log_e \left(\frac{1}{0.63}\right)$, which gives $C = 0.01\mu F$.

<table>
<thead>
<tr>
<th>Details of 2N2646</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number</strong></td>
</tr>
<tr>
<td>2n2646</td>
</tr>
</tbody>
</table>

**Waveforms:**

![Waveforms Diagram]

**Result:**
RC COUPLED AMPLIFIER
(With and without feedback)

Aim:
To design and set up an RC-coupled CE amplifier using bipolar junction transistor and to plot its frequency response.

Components and Equipments Required

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BC107</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>10 kΩ, 47kΩ, 680Ω, 47kΩ, 820Ω</td>
<td>5 No</td>
</tr>
<tr>
<td>3.</td>
<td>Capacitors</td>
<td>10µF, 22µF</td>
<td>2 No</td>
</tr>
</tbody>
</table>

Signal generator, dc power supply, CRO, etc

Theory:
RC-coupled CE amplifier is widely used in audio frequency applications in radio and TV receivers. It provides current, voltage and power gains. Base current controls the collector current of a common emitter amplifier. A small increase in base current results in a relatively large increase in collector current. Similarly, a small decrease in base current causes large decrease in collector current. The emitter-base junction must be forward biased and the collector-base junction must be reverse biased for the proper functioning of an amplifier. In the circuit diagram, an NPN transistor is connected as a common emitter ac amplifier. R1 and R2 are employed for the voltage divider bias of the transistor. Voltage divider bias provides good stabilization independent of the variations of β. The input signal V_in is coupled through C1 to the base and output voltage is coupled from collector through the capacitor C2.

The input impedance of the amplifier is expressed as $Z_{in} = R_1 || R_2 || ((1 + \beta)(r_e))$ and output impedance as $Z_o = \frac{R_c}{r_e} || R_L$, where $r_e$ is the internal emitter resistance of the transistor given by the expression $25 \text{ mV}/I_e$, where 25 mV is temperature equivalent voltage at room temperature.

When removing the bypass capacitor C_e, the negative feedback increases, hence the gain of the amplifier reduces. Also bandwidth of the amplifier increases, due to the reduction of a low frequency pole.

Circuit Diagram:
Procedure

1. Test all the components using a multimeter. Set up the circuit and verify dc bias conditions. To check dc bias conditions, remove input signal and capacitors in the circuit.
2. Connect the capacitors in the circuit. Apply a 100 mV peak to peak sinusoidal signal from the function generator to the circuit input. Observe the input and output waveforms on the CRO screen simultaneously.
3. Keep the input voltage constant at 100 mV, vary the frequency of the input signal from 0 to 1 MHz or highest frequency available in the generator. Measure the output amplitude corresponding to different frequencies and enter it in tabular column.
4. Plot the frequency response characteristics on a graph sheet with gain in dB on y-axis and log(f) on x-axis. Mark log f_L and log f_H corresponding to 3 dB points. (If a semi-log graph sheet is used instead of ordinary graph sheet, mark f along x-axis instead of log f).
5. Calculate the bandwidth of the amplifier using the expression BW = f_H - f_L:
6. Remove the emitter bypass capacitor C_E from the circuit and repeat the steps 3 to 5 and observe that the bandwidth increases and gain decreases in the absence of C_E.

Design:

- **Output requirements**: Mid-band voltage gain of the amplifier A_V = 50 and required output voltage swing = 10 V.
- **Selection of transistor**: Transistor is selected according to the frequency of operation, and power requirements. The h FE (β_ac) of the transistor is another aspect we should be careful about. Low frequency gain of a BJT amplifier is given by the expression. h FE (β_ac) of any transistor will vary in large ranges. For example, the h FE of SL100 (a general purpose transistor) varies from 40 to 300. h FE of BC107 (an AF driver) varies from 100 to 500. Therefore a transistor must be selected such that its minimum guaranteed h FE is greater than or equal to A_V required.
  Select transistor BC107 since its minimum guaranteed h FE (= 100) is more than the required gain (=50) of the amplifier.

Quick Reference data of BC107

Type: NPN-Silicon, Application: In audio frequency
Maximum rating: V CB = 50 V, V CE = 45 V, V EB = 6 V, I C = 100 mA.
Nominal rating: V CE = 5 V, I C = 2 mA, h FE = 100 to 500.

- **DC biasing conditions**: VCC is taken as 20% more than required output swing. Hence VCC = 12 V. IC = 2mA, because h FE is guaranteed 100 at that current as per data sheet.
  In order to make the operating point at the middle of the load line, assume the dc conditions V RC = 40% of V CC = 4.8 V, V RE = 10% of V CC = 1:2 V and V CE = 50% of V CC = 6 V.
- **Design of R C**:
  \[ V_{RC} = I_C R_C = 4.8 \text{ V} \]
  From this, we get R C = 2.4 kΩ. Use 2.2 k as standard.
- **Design of R E**:
  \[ V_{RE} = I_E R_E = 1.2 \text{ V} \]
  From this, we get R E = 600 Ω because I E = I C. Use 680Ω as std.
- **Design of voltage divider R1 and R2**:
  Assume the current through R 1 = 10I b and that through R 2 = 9I b for a stable voltage across R 1 and R 2 independent of the variations of the base current
  \[ V_{R2} = \text{Voltage drop across } R_2 = V_{BE} + V_{RE} \]
  i.e.,
  \[ V_{R2} = 0.6 + 1.2 = 1.8 \text{ V} \]
Also,
\[ V_{R2} = 9I_B R_2 = 1.8V, \] But \( I_B = I_c / h_{ie} = 2 \text{ mA} / 100 = 20 \mu A. \)

Then
\[ R_2 = \frac{1.8V}{9 \times 20 \mu A} = 10 \Omega \]

Similarly
\[ V_{R1} = \text{Voltage drop across } R_2 = V_{CC} - V_{R2} = 12 - 1.8 = 10.2V \]

Also,
\[ V_{R1} = 10I_B R_1 = 10.2V, \] where \( I_B = 20 \mu A. \)

Then
\[ R_1 = \frac{10.2V}{10 \times 20 \mu A} = 51 \Omega \] (use 47 k\Omega as std)

- **Design of \( R_L \):** Gain of the common emitter amplifier is given by the expression, \( A_v = -\frac{(R_c || R_L)}{r_e}. \) where \( r_e = 25 \text{ mV/I}_e = 25 \text{ mV/2 mA} = 12.5 \Omega. \) Since the required gain = 50, substituting it in the above expression \( |A_v| = \frac{R_c || R_L}{r_e} = 50, \) Solving this expression, we will get \( R_L = 845 \Omega. \) Use 820 \Omega std.

- **Design of coupling capacitors \( C_{C1} \) and \( C_{C2} \):** \( X_{C1} \) should be less than the input impedance of the transistor. Here, \( R_{in} \) is the series impedance. Then \( X_{C1} \leq R_{in} / 10. \) Here \( R_{in} = R_1 || R_2 || (1 + \beta)(\tau_e) \) because is RE bypassed. Substituting the values of components we get \( R_{in} = 1.1 \text{ k}\Omega. \) Then \( X_{C1} \leq 110 \Omega. \) So, \( C_{C1} \geq \frac{1}{2\pi f_L \times 110} = 14.47 \mu F. \) Use 15 \mu F std, where \( f_L = 100Hz. \) Similarly \( X_{C2} \leq R_{out} / 10, \) where \( R_{out} \) is the resistance looking from the output terminals of the amplifier which is equal to \( R_C. \)

Hence, \( X_{C2} \leq \frac{R_C}{10} = 220 \Omega. \) Hence \( C_{C2} \geq \frac{1}{2\pi f_L \times 220} = 7.23 \mu F, \) use 10 \mu F std.

- **Design of bypass capacitor \( (C_e) \):** The design of \( C_e \) is such that \( X_{C1} \leq R_C / 10 = 68 \Omega, \) from this we will get,
\[
C_{C1} \geq \frac{1}{2\pi f_L \times 68} = 23.4 \mu F. \] Use 22 \mu F standard.

**Observation and graph:**

<table>
<thead>
<tr>
<th>Tabular Column</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f ) (Hz)</td>
</tr>
<tr>
<td>----------------</td>
</tr>
</tbody>
</table>

**Troubleshooting**

1. Before the ac signal is applied, check dc conditions of the amplifier. Ensure that the transistor is in active region by verifying that the E-B junction is forward biased and C-B junction is reverse biased.
2. Replace RE by a pot and connect the bypass capacitor at the variable terminal of the pot. Verify whether \( V_{BE} = 0.6 \text{ V}. \) This is very important.
3. If the output waveform gets clipped, reduce the amplitude of the input signal, vary \( R_C \) or adjust \( V_{CC} \) slightly.
4. If the voltage at the collector \( V_C = 12 \text{ V}, \) collector circuit is not drawing current. Transistor is in cut off state. Base-emitter junction may not be forward biased.
5. If \( V_C = 0, \) possible trouble is open collector circuit or collector shorted to earth. If \( V_C = 0, \) emitter is drawing current.

**Result:**
EMITTER FOLLOWER or COMMON COLLECTOR AMPLIFIER
(with and without complementary transistors)

Aim:

Design and test a common collector current amplifier and find the following parameters

1. Current gain
2. Voltage gain
3. Bandwidth
4. Input and output impedance

Components and Equipments Required

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BC107, BC177</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>33kΩ, 27kΩ</td>
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<tr>
<td>3.</td>
<td>Capacitors</td>
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<td>1 No.</td>
</tr>
<tr>
<td></td>
<td>Signal generator, dc power supply, CRO, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory:

Emitter follower is a popular name for common-collector amplifier. It is used as a current amplifier (buffer). Its voltage gain is approximately unity; current gain and power gain are much greater than unity. It is called the common-collector configuration because (ignoring the power supply battery) both the signal source and the load share the collector lead as a common connection point as in figure. Output is taken from the emitter terminal with respect to ground. This output voltage is in phase and is approximately equal to the input voltage.

It should be apparent that the load resistor in the common-collector amplifier circuit receives both the base and collector currents, being placed in series with the emitter. Since the emitter lead of a transistor is the one handling the most current (the sum of base and collector currents, since base and collector currents always mesh together to form the emitter current), it would be reasonable to presume that this amplifier will have a very large current gain. This presumption is indeed correct: the current gain for a common-collector amplifier is quite large, larger than any other transistor amplifier configuration.

The name emitter follower came from the fact amplitude and phase of the signal at the output follows signal at the base. By virtue of high input impedance and low output impedance of this amplifier configuration, it is useful for impedance matching applications.

Voltage divider biasing is commonly used to bias emitter follower. Here \( R_E \) functions as a load resistance as well as a feedback resistance. This circuit uses voltage series feedback.

The input impedance of the amplifier is

\[
Z_{in} = R_1 || R_2 = R_1 || R_2 || \left( \frac{1 + \beta}{R_E + r_e} \right) \approx R_1 || R_2 || \left( \beta \right) R_E. \quad \text{(Very high)}
\]

The output impedance is

\[
Z_{out} = R_E || r_e \approx r_e, \text{ where } r_e = \frac{V_T}{l_E} = \frac{25mV}{l_E}
\]
Voltage gain of CC configuration is, \[ A_V = \frac{R_E}{R_E + r_E} \approx 1, \] and

Current gain \[ |A_I| = A_V \frac{R_1}{R_E} \text{ or } |A_I| = A_V \frac{R_1 |R_2|}{R_1 |R_2| + R_b} \]

In Fig 2 is a complementary symmetry emitter follower circuit, in which two transistors—an npn and a pnp—are used. In the positive half cycle of the a.c input voltage transistor Q1(npn) will be in active region and Q2(pnp) will be in cut-off region. Similarly in the negative half cycle of input, Q2 conducts more than Q1. This type of biasing is called class B arrangement. Here, Q1 or Q2 starts conducting only if the magnitude of the input voltage is greater than the base emitter voltage (0.7V), hence the output will be distorted (crossover distortion). In order to avoid the cross over distortion, two silicon diodes are connected in series, at the bases of Q1 and Q2, as shown in Fig 3. By connecting these two diodes, the base emitter voltages of each transistor are clamped to 0.7V, i.e., the base to base voltage is 1.4V. This type of biasing is called class AB biasing. The advantages of this circuit are increased input impedance and very low output resistance than that of an emitter with single transistor. Besides these, the power dissipation across the transistor get reduced by one half that with single transistor.

Circuit diagram:
Design:

a. Without complementary transistor.

Selection of transistor:
Select BC107, low frequency silicon transistor. DC current gain ($\beta$) $\cong 100$.

Supply voltage ($V_{cc}$):
Take $V_{cc}$ as 20% more than the maximum output voltage swing. Let the maximum voltage swing be 10V, then $V_{cc} = 10V + 20\% \times (10V) = 12V$

DC bias conditions:
We have $V_{ce} = 12V$, take $V_{ce} = 50\% \times V_{ce} = 6V$, to make the Q-point at the middle of the load line.

Selection of $R_E$:
By taking KVL,
\[ V_{RE} = V_{CC} - V_{CE} = 12 - 6 = 6V. \]
Now,
\[ R_E = \frac{V_{CE}}{I_E} = \frac{6V}{2mA} = 3k\Omega, \text{ (select 3.3k$\Omega$ standard), where } I_E = I_C = 2mA. \]

Selection of $R_1$ and $R_2$:
For better stability the current through $R_2$ ($I_{R2}$) $\gg$ the base current $I_B$. Let current through $I_{R1} = 10I_B$, then
\[ I_{R2} = 9I_B, \text{ where } I_B = \frac{I_C}{\beta} = \frac{2mA}{100} = 20\mu A. \]
Taking KVL at the base loop,
\[ V_{R1} = V_{BE} + V_{RE} = 0.7 + 6 = 6.7V. \]
Then
\[ R_2 = \frac{V_{R2}}{I_{R2}} = \frac{6.7V}{180\mu A} = 36.6k\Omega \text{ (select 33k$\Omega$ standard).} \]
Also from the circuit it is clear that,
\[ V_{R2} = V_{CC} - V_{R1} = 12 - 6.6 = 5.4V \]
Then,
\[ R_1 = \frac{V_{R1}}{I_{R1}} = \frac{5.4V}{10I_B} = \frac{5.4V}{200\mu A} = 27k\Omega \text{ (select 22k$\Omega$ standard).} \]

Design of coupling capacitors ($C_{c1}$ and $C_{c2}$):
The rule for designing coupling capacitor $X_{C1} \leq \frac{R_{in}}{10}$
\[ X_{C1} \leq \frac{R_1 || R_2 || (1 + \beta)(R_E + R_2)}{10} = 1.27k\Omega. \]
Or
\[ C_1 \geq \frac{1}{2nfL \times X_{C1}} = \frac{1}{2 \times 3.14 \times 100 \times 1.27 \times 10^3} = 1.25\mu F \text{ (select 1$\mu$F), (by assuming } f = 100Hz). \]
Take $C_{c2} = C_{c1} = 1\mu F$ (Because $C_{c2}$ acts as the input coupling capacitor of the next stage).

b. With complementary transistors

Selection of transistors:
As in previous case, select BC107-npn transistor and its complementary BC177 pnp transistor.

DC bias conditions:
\[ V_{CE1} = V_{CE2} = 50\% V_{cc} = 6V. \]
\[ V_{BB} = V_{BB1} - (V_{BB2}) = 0.7 + 0.7 = 1.4V. \]

Design of $R_1$ and $R_2$:
\[ V_{R1} + V_{R2} = V_{CC} - V_{BB} = 12 - 1.4 = 10.6V \]
Hence $V_{R1} = V_{R2} = V_{BB} = 5.3V,$
But we know that, for better stability, or for a stable Q point, $I_{r1}=10I_{n1}$, and also $I_{r2}=10I_{n2}$ where $I_{n}=I_{c}/\beta=2mA/100=20\mu A$.

i.e., $R_1=R_2=V_{r}/10I_{n}=26.5k\Omega$, and $R_1=R_2=33k\Omega$ standard.

**Design of coupling capacitors:**

Design of coupling capacitors are same as that in previous design. $C_{c1}=C_{c2}=C_{c3}=1\mu F$.

**Tabular Column and Graph**

<table>
<thead>
<tr>
<th>F in Hz</th>
<th>Vo in Volts</th>
<th>Gain in(dB)</th>
</tr>
</thead>
</table>

**Procedure**

1. Connect the circuit as per the circuit diagram
2. Check the biasing conditions.
3. Feed $V_{in}=5V_{pp}$ sine wave as input from the signal generator
4. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz(10, 50, 100, 500, 1KHz, 5KHz, 10KHz, 50KHz, ......1MHz, 2MHz) and note down the corresponding output voltages.
5. Plot the gain (dB) vs frequency.
6. Calculate the bandwidth from the graph
7. Find the input and output impedances. (Set the input frequency 3KHz to 10KHz range.)

**To find input impedance:**

b. Connect a 10kΩ resistance in series with the input signal source.

c. By using a multimeter measure the voltage across ($V'$) the 10k resistance, then find $I_{in}=V'/10k$.

d. The peak value of the voltage across the 10k resistance is $\sqrt{2}V'$. then the input voltage at the amplifier input ($V_{in}$) is $V_{in}=V'$.

e. Find $R_{in}, R_{in}=V_{in}/I_{in}$ (compare with theoretical value)

**To find the output resistance**

b. Connect a 1k pot across the output terminals. By varying the pot, set the output voltage half of that obtained without the pot.

c. Remove the pot, and measure the resistance across the terminals of the pot. (Compare with the theoretical value).
8. Note down the phase angle, bandwidth, and voltage gain ($A_v$).
9. To find the current Gain, $|A_i|=A_v \cdot R_{in}/r_e$.
10. Repeat the same procedures with complementary transistor emitter follower circuit.

**Result:**
CASCODE AMPLIFIER

Aim:
To design and set up a cascade amplifier and to draw its frequency response graph.

Components and equipments required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BC107</td>
<td>2 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>330Ω, 680Ω, 1.2 kΩ, 12 kΩ, 22 kΩ, 33kΩ</td>
<td>6 No</td>
</tr>
<tr>
<td>3.</td>
<td>Capacitors</td>
<td>2.2µF, 2.2µF, 22µF</td>
<td>3 No.</td>
</tr>
<tr>
<td></td>
<td>Signal generator, Multimeter, DC power supply, CRO, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory
A cascode amplifier comprises of a common emitter and common base amplifier stages in cascade. In the circuit diagram shown in figure, transistor T2 is in CE configuration and T1 in CB configuration. Principal advantages of this circuit is its low input capacitance which is a limiting factor of voltage gain at high frequencies. Cascode amplifier is able to amplify wider range of frequencies than that are possible with CE amplifiers. This is because no high frequency feedback occurs from the output back to the input through the miller capacitance as it occurs in transistor CE configuration. Cascade amplifier provides same voltage gain of CE amplifier but in wide range of frequencies. The transistors must be identical for good performance of cascode amplifier. The advantage of CE and CB stages are put together in cascode connection. The transistor must be identical for good performance of amplifier.

Circuit Diagram:
Design:

Output requirements: $V_o = 12V_{pp}$, $A_v = 20$

Selection of Transistor: Select BC107 as transistor $T_1$ and $T_2$.

DC biased condition:

$V_{cc} = 12V, I_c = 2mA, V_{CE1} = V_{CE2} = 35\%$ of $V_{cc} = 4.2V, V_{RE} = 10\%$ of $V_{cc} = 1.2V, V_{RC} = 20\%$ of $V_{cc} = 2.4V$

Design of $R_E$: $V_{RE} = I_c R_E = 1.2V \quad R_E = 600\Omega$. Use 560\Omega std.

Design of $R_C$: $V_{RC} = I_c R_C = 2.4 \quad \text{Then } R_C = 1.2k$

Design of $R1$ and $R2$ and $R3$:

We know from the circuit, $V_{CC} = V_{R1} + V_{BE1} + V_{CE2} + V_{RE}$

Or, $V_{R1} = 12 - 0.6 - 4.2 - 1.2 = 6V$

Also, for a stable Q point, we take

$I_{R1} = 10I_B$, where, $I_B = I_c / h_{fe} = 20\mu A$, \quad $\therefore R_1 = V_{R1} / I_{R1} = 6/10I_B = 6V/(10 \times 20\mu A) = 30k \quad \text{use 33k}\Omega$

By taking KVL,

$V_{R2} = V_{CC} - (V_{R1} + V_{BE2} + V_{RE}) = 12-(6+0.6+1.8) = 4.2V$

From the circuit it is clear that, $I_{R2} = 9I_B$, \quad $\therefore R_2 = V_{R2} / I_{R2} = 4.2V/180 \mu A = 23.3k\Omega$, use 22k\Omega as std.

Also, $V_{R3} = V_{CE} + V_{BE2} = 1.2+0.6 = 1.8V$, and $I_{R3} = 8I_B$

$\therefore R_3 = V_{R3} / I_{R3} = 11.2k\Omega$. Use 12 k\Omega std.

Design of $R_L$:

$A_v = \frac{g_m (R_C || R_L)}{h_{fe} R_E}$, But $g_m = I_c / V_i = 2mA / 26mV$, \quad $\therefore R_L = 330\Omega$

Selection of coupling capacitors $C_{C1}$, $C_{C2}$, $C_{C3}$:

The rule of coupling capacitor is $X_{C1} \leq R_{in}/10$. Here $R_{in} = R_2 || R_3 || h_{fe} R_E$

We get $R_{in} = 7k$, then $X_{C1} \leq 0.7k$. So, $C_{C1} \leq \frac{1}{2\pi f_L \times 0.7k} = 2.2\mu F$.

Assuming $f_L = 100Hz$. Take $C_{C1} = C_{C2} = C_{C3} = 2.2\ \mu F$

Selection of bypass capacitors $C_E$:

To bypass the lowest frequency (say 100Hz), $X_C \leq R_E/10$. Then $C_E \leq \frac{1}{2\pi f_L \times 60} = 26\mu F$. Use 26\mu F std.

Observation and graph:

<table>
<thead>
<tr>
<th>F in Hz</th>
<th>Vo in Volts</th>
<th>Gain in(dB)</th>
</tr>
</thead>
</table>

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**Procedure:**

1. Test all the components and verify the dc conditions.
2. Apply a 100 mV sinusoidal signal from the signal generator to the circuit input. The amplitude of the sinusoidal signal must be 100 mV peak to peak. Observe the input and output wave forms on a dual trace CRO screen.
3. Keep the input amplitude constant, vary the frequency of the input signal Hz to a few MHz and note down corresponding output amplitude from CRO and enter it in the table.
4. Plot the frequency response characteristics.
5. Calculate the bandwidth of the amplifier using the expression $BW = f_H - f_L$.

**Result:**
CLASS-A POWER AMPLIFIER

Aim:

To set up and study the working of a series-fed Class- A audio power amplifiers.

Components and Equipments Required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>SL100</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>33Ω, 2.2kΩ</td>
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<tr>
<td>3.</td>
<td>Capacitors</td>
<td>220µF</td>
<td>2 No.</td>
</tr>
<tr>
<td></td>
<td>Signal generator, dc power supply, CRO, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory:

A class-A power amplifier is defined as a power amplifier in which output current flows for the full-cycle (360°) of the input signal. In other words, the transistor remains forward biased throughout the input cycle.

A schematic circuit of a series fed class A large signal amplifier using resistive load \( R_c \) is shown below. The term “series fed” is derived from the fact that the load \( R_c \) is connected in series with the transistor output. The only difference between this circuit and the small-signal amplifier circuits is that the signals handled by the large-signal circuit are in the range of volts and the transistor used is a power transistor capable of operating in the range of a few watts. This circuit is seldom used for power amplification because of its poor collector efficiency but will give clear understanding of class A operation to the readers. The output characteristics with operating point Q are also shown. \( I_{CQ} \) and \( V_{CEQ} \) represent no signal collector current and collector-emitter voltage respectively. When ac input signal is applied, the operating point Q shifts up and down causing output current and voltage to vary about it. The output current increases to \( I_{c \text{ max}} \) and falls to \( I_{c \text{ min}} \). Similarly, the collector-emitter voltage increases to \( V_{ce \text{ max}} \) and falls to \( V_{ce \text{ min}} \).

The efficiency of series-fed class-A amplifier is, \( \eta = \frac{P_o}{P_i} \), where \( P_o \) is the output (ac) power, \( P_i = \frac{V_{CEQ}^2}{2R_c} \)

and \( P_i \) is the input (dc) power given by, \( P_i = V_{CE}I_{CQ} \).

The maximum efficiency, \( \% \eta_{\text{max}} = 25\% \).

Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%. Because of this reason, series-fed amplifier is seldom used. Another type of class-A amplifier having maximum efficiency of 50% is transformer coupled class A amplifier.

Design:

Required output power, \( P_o = 250 \text{mW} \) for a given load of 33Ω.

Selection of transistor:

Select power transistor SL100.
DC bias voltage:

We have, \[ P_o = \frac{V_{CE(p)}}{2R_c} = 250mW, \]  where \( R_c = R_L = 33\Omega \).

\[ \therefore V_{CE} = 4.06V, \]

Also we have, \( V_{CC} > V_{CE(pp)} \), or \( V_{CC} > 2 \times 4.06V = 8.1V \). Set \( V_{CC} = 9V \).

Selection of \( R_B \)

From the circuit, \[ V_{CE} = V_{CC} - I_c R_C, \]  or \[ I_c = \frac{1}{R_c} (V_{CC} - V_{CE}) = \frac{1}{33} (9 - 4.06) = 149.6mA \]

\[ \therefore I_B = \frac{I_c}{\beta} = \frac{149.6mA}{40} = 3.74mA, \]  where \( \beta = 40 \).

Also, \[ R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{9 - 0.6}{3.74mA} = 2.2k\Omega. \]

Selection of coupling capacitors:

\( R_C C_C >> T_s \), where \( f_s = 1/T_s \) is the lowest signal frequency (20Hz).

Hence \[ C_C = \frac{1}{2\pi f_s R_L} = 241.2\mu F. \]  Use 220\mu F std.

Circuit Diagram:

Waveforms:

Q-point of Class-A amplifier.

Output of class-A amplifier

Result:
CLASS-B AND CLASS-AB POWER AMPLIFIER

Aim:
To set up and study the working of a complementary symmetry class-B and class AB push pull audio power amplifiers.

Components and Equipments Required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
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<td>Diodes</td>
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<td>2 No.</td>
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</table>

Signal generator, dual power supply, CRO, etc

Theory:
Class B operation means that the Q point is located at the cut-off and hence collector current flows for 180° of the input cycle. A complementary symmetry circuit uses two complementary pair transistors NPN and PNP with identical characteristics. Both the transistors are connected as emitter follower in push pull arrangement. The name push pull comes from the fact that one transistor drives current through the load in one direction while the other transistor drives current in opposite direction. This type of amplifiers do not need input transformer for phase splitting. Thus the cost and bulkiness of the circuit is reduced.

During the positive half cycle of the input, base of npn transistor T2 is driven positive relative to its emitter. This makes the transistor conducts. At the same time, other transistor remains in OFF state. During the negative half cycle of the input, transistor T1 conducts and T2 becomes OFF. Now, output current flows in the opposite direction. Voltage developed across Rl is same as the input voltage because gain of the amplifier is unity.

There is a great chance of thermal runaway due to the sensitivity of collector current with temperature. Compensating diodes are used to avoid thermal runaway. Diode curves should match with the VBE curves of the transistor. Therefore the bias current through the diode must be same as that of the quiescent collector current. In class B power amplifier transistor will start conducting only after the input reaches 0.6V. This causes output voltage to distort near the zero crossing. This distortion is called cross over distortion. Cross over distortion can be eliminated by connecting a resistance in series with diodes. Voltage developed across this resistor drives transistor into class AB operation. This happens because the operating point moves towards class-A operating point slightly. A high value coupling capacitor is required to couple a low impedance at low frequency.

Procedure:
2. Set up the class-B amplifier circuit using dual power supply as shown in figure after testing all the components. Observe the cross over distortion on CRO screen shorting the diodes.
3. Apply a low frequency 2Vpp sine wave at the input and observe the input and output waveforms on the CRO screen. Calculate ac power delivered to the load using the expression \(V_{pp}^2 / 2R_L\).
4. Repeat the above steps for class-B power amplifier circuit using single power supply. Observe that the cross over distortion is still present slightly.
5. Repeat the experiment for class AB amplifier and observe that the cross over distortion is eliminated.
Circuit Diagrams:

a. Class B power amplifier using dual power supply.

b. Class B power amplifier using single power supply.

c. Class AB power amplifier.
*Electronic Circuit Lab Manual*

**Design:**

1. **Class B amplifier using dual power supply.**

   Required output power $P_o = 25 \text{ mV}$

   **Selection of Transistors:** Select SK100 as T1 & SL 100 as T2 as the matched pair transistor. 2N3055 and Mj2955 are also high power complementary pair transistors.

   **Selection of $R_L$:** Output power $\frac{V_p^2}{2R_L}$.

   Therefore $\frac{V_p}{V_m} = 1\text{V}$ because the amplifier is an emitter follower.

   **Design of coupling capacitors:**

   $R_L C >\gg T_s$, where $f_s = 1/T_s$ is the lowest signal frequency (20Hz).

   Hence $C_C = \frac{1}{2\pi \times 20R_L} = 360\mu F$. Use $470\mu F$ std.

2. **Class B power amplifier using single power amplifier:**

   Required output power $P_o = 25 \text{ mV}$

   **Selection of Transistors:** Select SK100 as T1 & SL 100 as T2 as the matched pair transistor. 2N3055 and Mj2955 are also high power complementary pair transistors.

   **Selection of diodes:** Select diodes 1N4001 since diodes and transistors should be made of same material because the diodes are compensating the $V_{BE}$ of transistors.

   **Selection of $R_L$:** Output power $\frac{V_p^2}{2R_L}$.

   Therefore $\frac{V_p}{V_m} = 1\text{V}$ because the amplifier is an emitter follower.

   **Design of R:** The bias current through the compensating diodes $I_D$ is same as the $I_{CQ}$ in order to match the diode curves and $V_{BE}$ curve of the transistor. $I_{CQ}$ should be 1 to 5% of collector saturation current $I_{C_{Sat}}$.

   Average current $I_{C_{Sat}} = \frac{V_{CEQ}}{\pi R_L} = \frac{3}{\pi R_L} = 43\text{mA}$. Let $R_1 = R_2 = R$

   $I_D = \frac{(V_{CC} - V_{BE})}{2R} = \frac{(6 - 1.2)}{2R}$.

   Since $I_{CQ} = I_D = 5\% I_{C_{Sat}} = 2.15\text{mA}$. Then $R = 1.1\text{ k}\Omega$. Use $1\text{ k}\Omega$ std.

   **Design of coupling capacitors:**

   $R_L C >> T_s$, where $f_s = 1/T_s$ is the lowest signal frequency (20Hz).

   Hence $C_C = \frac{1}{2\pi \times 20R_L} = 360\mu F$. Use $470\mu F$ std.

3. **Class AB power amplifier:**

   **Design of $R_L$ and $C_C$:** are same as that of class-B amplifier.

   **Design of R and $R_B$:**

   The bias current through the compensating diodes $I_D$ is same as the $I_{CQ}$ in order to match the diode curves and $V_{BE}$ curve of the transistor. $I_{CQ}$ should be 1 to 5% of collector saturation current $I_{C_{Sat}}$.

   Average current $I_{C_{Sat}} = \frac{V_{CEQ}}{\pi R_L} = \frac{3}{\pi R_L} = 43\text{mA}$. Let $R_1 = R_2 = R$

   $I_D = \frac{(V_{CC} - V_{BE})}{2R} = \frac{(6 - 1.2)}{2R}$.
Electronic Circuit Lab Manual

Since $I_{CQ} = I_D = 5\% I_{SAT} = 2.15\, mA$. $R = 1.1\, k\Omega$. Use 1kΩ std.

Applying KVL in the diode network, $6V = I_D \times 2R + 1.2V + I_D \times R_B$.

$I_D \times R_B$ should be about 2V to drive into class-AB.

$\therefore I_D \times R_B = 2V$, which gives, $R_B = 930\, \Omega$. Use 1kΩ std.

Waveforms:

Output of class-B amplifier with cross over distortion

Output of class-AB amplifier

Result:
ASTABLE MULTIVIBRATOR

Aim:
To design and set up an astable multivibrator using transistors, study its performance and observe the waveforms.

Components and equipments required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BC107</td>
<td>2 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>82kΩ, 4.7kΩ</td>
<td>4 No</td>
</tr>
<tr>
<td>3.</td>
<td>Capacitors</td>
<td>0.01µF, 0.022µF</td>
<td>2 No</td>
</tr>
<tr>
<td></td>
<td>DC power supply, CRO, etc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Theory:
Astable multivibrator is also called free running oscillator. It is used to generate square wave for a given frequency, amplitude and duty cycle. It does not have a stable state. Astable circuit switches back and forth between two quasi stable states depending upon the charging and discharging periods of two timing capacitors.

Suppose transistor Q₁ is OFF and transistor Q₂ is ON. Then the capacitor C₂ starts charging to Vcc through R₂ and Q₂. When the potential at left side of capacitor becomes the cut in voltage (0.4V), Q₁ starts conducting. Sudden surge of base current into Q₁ creates a momentary rise in base voltage. But soon it settles at 0.7 V. When Q₁ conducts, Q₂ goes to OFF state due to regenerative action. Thus the time duration in which Q₂ remains in ON state is given by the expression \( T₂ = 0.69R₂C₂ \). Sudden conduction of \( Q₂ \) causes a potential drop of \( I_{C2}R₂ \) at the collector of \( Q₂ \). This sudden change gets transferred to the base of \( Q₁ \), because capacitor acts as a short circuit for sudden changes. This creates a potential of 0.7V - \( I_{C1}R₁ \) at the right side of capacitor C₁. Now C₁ starts charging toward Vcc through R₁ and Q₁. When the potential at right side of capacitor becomes the cut in voltage (0.4V), Q₁ starts conducting. Resulted sudden voltage drop of \( I_{C1}R₁ \) transfers from collector of Q₁ to base of Q₂. The base potential of Q₂ is then 0.7V - \( I_{C2}R₂ \). This cycle repeats. Time duration in which Q₁ remains ON is given by the expression \( T₁ = 0.69R₁C₁ \).

If \( R₁ = R₂ = R \) and \( C₁ = C₂ = C \), then \( T₁ = T₂ = T = 0.69RC \). Now the duty cycle is \( \frac{1}{2} \) and the time period of the output square wave \( T = T₁ + T₂ = 1.38RC \).

Circuit Diagram:
**Design:**

- **Output Requirements**

  A square wave of amplitude 9V, frequency 1 kHz and duty cycle=1/3. Choose transistor BC107.

  Take $V_{cc}=9V$, since the required amplitude of the output Square wave is 9V.

  Design of $R_{C1}$ and $R_{C2}$:

  $$R_{C1} = \frac{V_{cc} - V_{CEsat}}{I_{C1}} = \frac{9-0.3}{2mA} = 4.35k\Omega$$, with $I_{C1}=2mA$, use 4.7kΩ std. Also take $R_{C1}=R_{C2}=4.7k\Omega$

- **Design of $R_1$ And $R_2$**

  The resistors $R_1$ and $R_2$ must be able to keep the transistors in saturation region.

  $I_{bmin}=I_C/h_{re}=2mA/100=20\mu A$.

  Consider an over-driving factor of 5, so that transistors will be indeed in saturation. Then actual base current $I_b=0.1mA$.

  $$R_1 = \frac{V_{cc} - V_{BEsat}}{0.1mA} = 83k\Omega$$, use 82kΩ std, also take $R_1=R_2$.

  $R_1$ and $R_2$ should be less than $h_{re}R_C$.

- **Design Of $C_1$ and $C_2$**:

  Given that $T=T_1+T_2=1ms$. Duty cycle of AMV is $D = \frac{T_1}{(T_1 + T_2)} = 1/3$, From this, $T_1\approx0.33ms$ and $T_2\approx0.33ms$.

  $$T_1 = 0.33ms = 0.69R_1C_1$$, then $C_1 = 0.006\mu F$. Use 0.01μF std.

  $$T_2 = 0.66ms = 0.69R_2C_2$$, then $C_2 = 0.012\mu F$. Use 0.022μF to make $C_2=2C_1$.

  Note: While designing $R$ and $C$, find the value of $R$ first and substitute it in the expression of $T$, to obtain $C$. Do not do in reverse order. Casual selection of capacitor value may lead to a large value of resistor which will not permit sufficient base current for the transistor.

**Waveforms:**

**Procedure:**

1. Verify the condition of all components, devices and probes.
2. Set up the circuit and observe the collector and base waveforms of both transistors.

**Result:**
RC PHASE SHIFT OSCILLATOR

Aim:
To design and set up an RC phase shift oscillator using BJT and to observe the sinusoidal output waveform

Components and equipments required:

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Components Details</th>
<th>Specification</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BC107</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>680Ω, 2.2 kΩ, (4.7kΩx2),4.7k pot,10kΩ</td>
<td>7 No</td>
</tr>
<tr>
<td>3.</td>
<td>Capacitors</td>
<td>0.01µF x3, 22µF x1, 1 µFx1</td>
<td>3 No.</td>
</tr>
</tbody>
</table>

DC power supply, CRO, etc

Theory:
An oscillator is an electronic circuit for generating an ac signal voltage with a dc supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements. An oscillator requires an amplifier, a frequency selective network, and a positive feedback from the output to the input. The Barkausen criterion for sustained oscillation is $A\beta = 1$ where $A$ is the gain of the amplifier and $\beta$ is the feedback factor. The unity gain means signal is in phase.

If a CE amplifier is used, with a resistive collector load there is a $180^\circ$ phase shift between the voltages at the base and collector. Feedback network between the collector and base must introduce an additional $180^\circ$ phase shift at a particular frequency.

In this, three sections of phase shift networks are used so that each section introduces approximately $60^\circ$ phase shift at resonant frequency. By analysis, resonant frequency $f$ can be expressed by the equation,

$$f = \frac{1}{2\pi RC\sqrt{(6 + 4R_c/R)}}$$

The 3 section RC network offers a $\beta$ of 1/29. Hence the gain of the amplifier should be 29. For this the requirement on the $h_{fe}$ of the transistor is found to be,

$$h_{fe} \geq 23 + 29(R/R_c) + 4(R_c/R)$$

The phase shift oscillator is particularly useful in the audio frequency range

Procedure:

1. Set up the amplifier part of Hartley oscillator on a breadboard. Check the DC conditions of the amplifier.
2. Complete the circuit connecting the feedback circuit and observe output sinusoidal waveform on CRO screen. Measure its amplitude and frequency.

Circuit Diagram:
**Design:**

**Output requirements:**

Sine wave with amplitude $10V_{pp}$ and frequency 1KHz.

**Design of the amplifier:** Select BC107. It can provide a gain more than 29 because its minimum $h_{FE}$ is 100.

**DC biasing conditions:** $V_{CC}$ is taken as 20% more than required output swing. Hence $V_{CC} = 12$ V and $I_c = 2mA$.

In order to make the operating point at the middle of the load line, assume the dc conditions $V_{ce} = 50\%$ of $V_{CC} = 6$ V, $V_{RC} = 40\%$ of $V_{CC} = 4.8$ V, and $V_{RE} = 10\%$ of $V_{CC} = 1.2$ V.

**Design of $R_c$:**

$$V_{RC} = I_cR_C = 4.8 \text{ V}. \text{ From this, we get } R_c = 2.4 \text{ k}\Omega. \text{ Use } 2.2 \text{ k} \text{ as standard.}$$

**Design of $R_e$:**

$$V_{RE} = I_eR_E = 1.2 \text{ V}. \text{ From this, we get } R_e = 600 \text{ } \Omega \text{ because } I_e = I_c. \text{ Use } 680\Omega \text{ as std.}$$

**Design of voltage divider $R_1$ and $R_2$:**

Assume the current through $R_1 = 10I_n$ and that through $R_2 = 9I_n$ for a stable voltage across $R_1$ and $R_2$ independent of the variations of the base current.

$$V_{R2} = Voltage\; drop\; across\; R_2 = V_{BE} + V_{RE}\; \text{i.e., } V_{R2} = 0.6 + 1.2 = 1.8 \text{ V},$$

Also, $$V_{R2} = 9I_BR_2 = 1.8V, \text{ But } I_n = I_c/h_{Fe} = 2 \text{ mA}/100 = 20 \mu\text{A.}$$

Then $$R_2 = \frac{1.8V}{9 \times 20 \mu\text{A}} = 10k\Omega$$

Similarly $$V_{R1} = Voltage\; drop\; across\; R_2 = V_{CC} - V_{R2} = 12 - 1.8 = 10.2V$$

Also, $$V_{R1} = 10I_BR_1 = 10.2V, \text{ where } I_n = 20 \mu\text{A.}$$

Then $$R_1 = \frac{10.2V}{10 \times 20 \mu\text{A}} = 51k\Omega \text{ (use } 47k\Omega \text{ as std).}$$

**Design of frequency selective network:**

Required frequency of oscillation is 1kHz.

$$f = \frac{1}{2\pi RC\sqrt{(6 + 4R_c/R)}} = 1kHz$$
Take $R = 4.7k\Omega$ to avoid loading of $R_c$ by the RC network. Then, $C = 0.01\mu F$. Use $4.7k\Omega$ pot in the last stage.

**Design of bypass capacitor ($C_E$):**

The design of $C_E$ is such that $X_{CE} \leq R_E/10 = 68\Omega$, from this we will get, $C_E \geq \frac{1}{2\pi f_L \times 68} = 23.4\mu F$. Use 22 $\mu F$ std.

**Waveform:**

![Waveform](image)

Output of phase shift oscillator

**Result:**
HARTLEY & COPITTS OSCILLATOR

Aim:
To design and set up Hartley and Colpitts oscillator for a given amplitude and frequency.

Components and equipments required:

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>1.</td>
<td>Transistor</td>
<td>BC107</td>
<td>1 No</td>
</tr>
<tr>
<td>2.</td>
<td>Resistors</td>
<td>1.2kΩ, 4.7kΩ, 47kΩ, 10kΩ</td>
<td>4 No</td>
</tr>
<tr>
<td>3.</td>
<td>Capacitors</td>
<td>0.01µF×2, 1µF×3</td>
<td>5 No.</td>
</tr>
<tr>
<td>4.</td>
<td>Inductors</td>
<td>5.6µH×2, 12µH.</td>
<td>2 No.</td>
</tr>
</tbody>
</table>
DC power supply, CRO, etc

Theory:
LC oscillators are preferred for high frequency generation. Hartley oscillators have LC tank circuit for frequency selection.

The voltage divider bias is used for the amplifier in CE configuration. Amplifier section provides 180° phase shift to signal current. The tank circuit provides another 180° phase shift to satisfy the Barkausen criterion. High frequency transistors are preferred for a better performance. R_e is bypassed by C_e to prevent ac signal degeneration and thus to improve the gain of the amplifier.

The Frequency of oscillation of Hartley oscillator is determined by the resonant circuit consisting of capacitor C and inductors L_1 and L_2.

\[ f = \frac{1}{2\pi \sqrt{(L_{eq} \cdot C)}} \]

where, \( L_{eq} = L_1 + L_2 \), since \( L_1 \) is in series with \( L_2 \).

The output voltage appears across \( L_1 \) and feedback voltage appears across \( L_2 \). So the feedback factor of the oscillator is given by \( \beta = L_2/L_1 \). This means that the gain of the amplifier section is \( A = L_1/L_2 \). This means that the \( h_{FE} \) of the transistor should be \( \geq L_1/L_2 \) for sustained oscillation.

Similarly the Frequency of oscillation of Colpitts oscillator is determined by the resonant circuit consisting of capacitor C and inductors L_1 and L_2. It is given by

\[ f = \frac{1}{2\pi \sqrt{(l_{eq} \cdot C)}} \]

where, \( l_{eq} = \frac{C_1 C_2}{C_1 + C_2} \), since \( C_1 \) is in series with \( C_2 \).

The output voltage appears across \( C_1 \) and feedback voltage appears across \( C_2 \). So the feedback factor of the oscillator is given by \( \beta = C_2/C_1 \). This means that the gain of the amplifier section is \( A = C_1/C_2 \). This means that the \( h_{FE} \) of the transistor should be \( \geq C_1/C_2 \) for sustained oscillation.
Circuit Diagrams

**Design:**

**Output requirements:** Sine wave of amplitude and frequency 100 KHz.

**Selection of transistor:** Use high frequency transistor BF 195. (BC107 can also be used because it is found to be working in frequency up to 1MHz)

Detail of BF 195:

- Type: Silicon, $V_{CE} = 10v$, $I_C = 1mA$, $h_{fe}$, typically = 50 to 125

**DC biasing conditions:**

$V_{CC}$ is taken as 20% more than required output swing. Hence $V_{CC} = 12$ V and $I_C = 1mA$. In order to make the operating point at the middle of the load line, assume the dc conditions $V_{CE} = 50\%$ of $V_{CC} = 6$ V. $V_{RE} = 40\%$ of $V_{CC} = 4.8$ V, and $V_{RE} = 10\%$ of $V_{CC} = 1.2$ V.

**Design of $R_C$:**

$V_{RC} = I_C R_C = 4.8 \text{ V}$. From this, we get $R_C = 4.8 \text{ k}\Omega$. Use 4.7 k as standard.
Design of $R_E$:

$$V_{RE} = I_E R_E = 1.2 \, V.$$ From this, we get $R_E = 1.2 \, k\Omega$ because $I_E = I_C$. Use $680 \, \Omega$ as std.

Design of voltage divider $R_1$ and $R_2$:

Assume the current through $R_1 = 10 I_B$ and that through $R_2 = 9 I_B$ for a stable voltage across $R_1$ and $R_2$, independent of the variations of the base current.

$$V_{R2} = \text{Voltage drop across } R_2 = V_{RE} + V_{RE}$$

i.e.,

$$V_{R2} = 0.6 + 1.2 = 1.8 \, V,$$

Also,

$$V_{R2} = 9 I_B R_2 = 1.8 \, V,$$

But $I_B = I_C/ h_{FE} = 1 \, mA/50 = 20 \, \mu A$.

Then

$$R_2 = \frac{1.8 \, V}{9 \times 20 \, \mu A} = 10 \, k\Omega$$

Similarly

$$V_{R1} = \text{Voltage drop across } R_1 = V_{CC} - V_{R2} = 12 - 1.8 = 10.2 \, V$$

Also,

$$V_{R1} = 10 I_B R_1 = 10.2 \, V,$$

where $I_B = 20 \, \mu A$.

Then

$$R_1 = \frac{10.2 \, V}{10 \times 20 \, \mu A} = 51 \, k\Omega \text{ (use } 47 \, k\Omega \text{ as std)}$$

Design of coupling capacitors: All capacitor values may take $1 \, \mu F$.

Design of feedback network:

a. Hartley oscillator:

All capacitor values may taken $1 \, \mu F$.

Required frequency of oscillation is $100 \, KHz$. We have, $f = \frac{1}{2 \pi \sqrt{(C_1 + C_2)L}} = 100 \, KHz$.

Take $C=0.01 \, \mu F$, then $L_1 + L_2 = 12.2 \, \mu H$. Take $L_1 = L_2 = 6.1 \, \mu H$. Use $5.6 \, \mu H$ fixed inductor.

b. Colpitts oscillator:

The frequency of oscillation is $f = \frac{1}{2 \pi \sqrt{(LC_{eq})}} = 100 \, KHz$, where $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$.

Let $C_1 = C_2 = 0.01 \, \mu F$. Then $L = 24.4 \, \mu H$. Use $22 \, \mu H$ std. Or use primary coil of IFT removing capacitor inside it.

Procedure:

1. Set up the amplifier part of Hartley oscillator on a breadboard.
2. Check the DC conditions of the amplifier.
3. Complete the circuit connecting the feedback circuit and observe output sinusoidal waveform on CRO screen. Measure its amplitude and frequency.
4. Repeat the above steps for Colpitts oscillator.

Waveforms:

![Waveform](image)

Output of phase shift oscillator

Result: